

REMARKS

By this Amendment, Applicants amend claims 1, 11, and 16. Claims 1-23 remain currently pending.

In the Office Action, the Examiner rejected claims 1-3, 5-7, 11-13, and 16-18 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,850,422 to Chen ("Chen") in view of Lee et al. ("An 84-mW 4-Gb/s Clock and Data Recovery Circuit for Serial Link Applications", VLSI Circuits Symposium Kyoto, Japan, June 2001) ("Lee"); rejected claim 4 under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of U.S. Patent Application Publication No. 2002/0030522 to Nakamura ("Nakamura"); rejected claims 8, 9, 15, 19, and 23 under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of U.S. Patent No. 7,113,560 to Huang et al. ("Huang"); rejected claims 21 and 22 under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Huang and Kim et al. ("Clock and data recovery circuit with two exclusive-OR phase frequency detector", Electronic Letters, Vol. 36, No. 16, 1347-1349, 3rd August 2000) ("Kim"); and rejected claims 10, 14, and 20 under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of U.S. Patent Application Publication No. 2003/0061564 to Maddux ("Maddux").¹

Applicants respectfully traverse the rejection of claims 1-3, 5-7, 11-13, and 16-18 under 35 U.S.C. § 103(a) as being unpatentable over Chen, because a *prima facie* case of obviousness has not been established.

¹ The Office Action contains a number of statements reflecting characterizations of the related art and the claims. Regardless of whether any such statement is identified herein, Applicants decline to automatically subscribe to any statement or characterization in the Office Action.

To establish a *prima facie* case of obviousness based on a combination or suggestion of prior art, “Office personnel must articulate . . . a finding that the prior art included each element claimed, although not necessarily in a single prior art reference, with the only difference between the claimed invention and the prior art being the lack of actual combination of the elements in a single prior art reference.” M.P.E.P. § 2143.A (8th edition, revision 6).

Independent claim 1, as amended,² recites a combination including, for example, “the phase detector provides to the encoder one set of oversampled data while oversampling at transition phases of the transmitted serial data and provides to the encoder two sets of oversampled data while oversampling at non-transition phases of the transmitted serial data.” Chen fails to teach or suggest at least these features of amended claim 1.

Chen teaches that “[t]he data sampler 14 uses the data on line 46 to sample the multiple clock phases P0-P9 during an initial phase acquisition period. . . . [T]he data on line 46 is used by the D flip-flops 40 to strobe the ten clock phases P0-P9. The first high-to-low transition of the data on line 46 causes one of the AND gates 42 to switch from logic 0 to logic 1. Subsequently, one of the output signal lines, OP0-OP9 switches from logic 0 to logic 1 after the second high-to-low transition of the data on line 46.” Chen, column 4, lines 54-65, emphasis added. However, Chen’s teaching of using the data as a strobe signal to provide phase transition does not constitute “the phase detector provides to the encoder one set of oversampled data while oversampling at transition phases of the transmitted serial data and provides to the encoder two sets of

² Support for the amendments may be found at, for example, paras. [023]-[026], of the specification.

oversampled data while oversampling at non-transition phases of the transmitted serial data,” as recited in amended claim 1 (emphasis added).

Further, Chen is silent on providing oversampled data based on oversampling conditions. In fact, Chen’s teaching of using data as a strobe signal for clock phase acquisition is entirely different from “the phase detector provides to the encoder one set of oversampled data while oversampling at transition phases of the transmitted serial data and provides to the encoder two sets of oversampled data while oversampling at non-transition phases of the transmitted serial data,” as recited in amended claim 1 (emphasis added).

Lee fails to cure the deficiencies of Chen. Lee teaches “[a] 4Gb/s serial link tracking clock and data recovery (CDR) circuit fabricated in 0.24μm CMOS technology dissipates 84mW and occupies 0.3mm².” Lee, Abstract. However, Lee fails to teach or suggest at least “the phase detector provides to the encoder one set of oversampled data while oversampling at transition phases of the transmitted serial data and provides to the encoder two sets of oversampled data while oversampling at non-transition phases of the transmitted serial data,” as recited in amended claim 1 (emphasis added).

Therefore, neither Chen nor Lee, taken alone or in any reasonable combination, teaches or suggests all claim elements amended claim 1. A *prima facie* case of obviousness has not been established. Accordingly, Applicants respectfully request withdrawal of the Section 103 rejection of amended claim 1. Because claims 2, 3, and 5-7 depend from claim 1, either directly or indirectly, Applicants also request withdrawal of the Section 103 rejection of claims 2, 3, and 5-7.

Further, amended independent claims 11 and 16, while of different scope, include similar recitations to those of amended claim 1. Claims 11 and 16 are therefore also allowable for at least the same reasons stated above with respect to amended claim 1. Applicants respectfully request withdrawal of the Section 103 rejection of amended claims 11 and 16 and claims 12-13 and claims 17-18, which depend from claims 11 and 16, respectively.

Applicants respectfully traverse the rejection of claim 4 under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Nakamura, because a *prima facie* case of obviousness has not been established.

Claim 4 depends from amended claim 1. Nakamura also fails to cure the deficiencies of Chen. The Examiner alleges that “Nakamura teaches of an oversampling clock recovery circuit (title of invention) where a relatively small number of clocks are supplied, and controlled in phase by a phase control circuit.” (Office Action at 7.) Even assuming the Examiner’s allegation is correct, which Applicants do not concede, Nakamura fails to teach or suggest at least the above listed elements recited in amended claim 1 and required by claim 4.

Therefore, neither Chen nor Nakamura, taken alone or in any reasonable combination, teaches or suggests all elements required by claim 4. A *prima facie* case of obviousness has not been established. Accordingly, Applicants respectfully request withdrawal of the Section 103 rejection of claim 4.

Applicants respectfully traverse the rejection of claims 8, 9, 15, 19, and 23 under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Huang; the rejection of claims 21 and 22 under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of

Huang and Kim; and the rejection of claims 10, 14, and 20 under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Maddux. Claims 8-10 and 21-23 depend from amended claim 1, claims 14 and 15 depend from amended claim 11, and claims 19 and 20 depend from amended claim 16. Huang, Kim, and Maddux are not cited by the Examiner for the features of Applicants' independent claims 1, 11, and 16 discussed above, and Applicants do not accede to the Examiner's characterization of these cited references. Applicants further submit that Huang, Kim, and Maddux also fail to cure Chen's deficiencies in teaching all claim elements of amended claims 1, 11, and 16, as explained in previous sections. Thus, claims 8-10, 14, 15, and 19-23 are also allowable for at least being dependent on an allowable base claim. Accordingly, Applicants respectfully request withdrawal of the Section 103 rejections of claims 8-10, 14, 15, and 19-23.

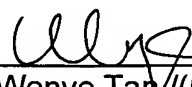
In view of the foregoing amendments and remarks, Applicant respectfully requests reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

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